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NOTICE OF ALLOWANCE AND FEE(S) DUE

34313 7590 05/10/2010

ORRICK, HERRINGTON & SUTCLIFFE, LLP
IP PROSECUTION DEPARTMENT
4 PARK PLAZA
SUITE 1600
IRVINE, CA 92614-2558

EXAMINER	
EL CHANTI, HUSSEIN A	
ART UNIT	PAPER NUMBER
2457	

DATE MAILED: 05/10/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,537	07/03/2003	Michael R. Butts	700693-4022	9026

TITLE OF INVENTION: SYSTEM AND METHOD FOR PERFORMING DESIGN VERIFICATION

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	08/10/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

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10/614,537	07/03/2003	Michael R. Butts	700693-4022	9026

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nonprovisional	NO	$1510	$300	$0	$1810	08/10/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
EL CHANTI, HUSSEIN A	2457	709-227000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 1152 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 1152 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/614,537	BUTTS ET AL.	
	Examiner	Art Unit	
	HUSSEIN A. EL CHANTI	2457	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/26/2010*.

2. ☒ The allowed claim(s) is/are *1-29*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Hussein Elchanti/ Primary Patent Examiner	

DETAILED ACTION

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Jeffrey Miller on May 3, 2010.

2. The application has been amended as follows:

1. (Currently amended) A co-verification interface, comprising a hardware component of a design verification system, a software component of the design verification system modeling the hardware component and being stored on a storage device, or a combination of the hardware and software components, the co-verification interface further comprising:

an application layer having a plurality of communication connections configured to communicate with a first system element of [a] the design verification system, wherein the design verification system performs functional verification of at least two system elements of a logic design including the first system element and a second system element;

a network layer in communication with said plurality of communication connections and being configured to select a communication connection from said plurality of communication connections;

a data link layer having a communication connection in communication with said selected communication connection and being configured to communicate with said network layer to provide flow control for said communication connection of said data link layer; and

a physical layer having a communication path in communication with said communication connection of said data link layer and being configured to communicate with the second system element of the design verification system only via the communication system,

wherein the first system element and the second system element are either a physical system element or a virtual system element, and

wherein the physical system element comprises one or more electronic components and the virtual system element comprises software models of the physical system element.

21. (Currently amended) A co-verification ~~interface implemented in~~ comprising a hardware component of a design verification system, a software component modeling the hardware component and being stored on a storage device of the design verification system, or a combination of the hardware and software components, the co-verification interface further comprising:

a first application layer having a plurality of communication connections configured to communicate with a physical system element, wherein the design verification system performs functional verification of at least two system elements of a logic design including the physical system element and a virtual system element;

a first network layer in communication with said plurality of communication connections of said first application layer and being configured to select a first communication connection from said plurality of communication connections of said first application layer;

a first data link layer having a communication connection in communication with said first communication connection and being configured to communicate with said first network layer to provide flow control for said communication connection of said first data link layer;

a second application layer having a plurality of communication connections configured to communicate with the virtual system element;

a second network layer in communication with said plurality of communication connections of said second application layer and being configured to select a second communication connection from said plurality of communication connections of said second application layer;

a second data link layer having a communication connection in communication with said second communication connection and said communication path and being configured to communicate with said second network layer to provide flow control for said communication connection of said second data link layer; and

a physical layer having a communication path in communication with said communication connection of said first data link layer and with said communication connection of said second data link layer, wherein the physical system element and the virtual system element communicate only via the physical layer,

wherein the physical system element comprises one or more electronic components and the virtual system element comprises software models of the physical system element.

22. (Currently amended) A design verification system comprising:

a first system element of a logic design;

a second system element of the logic design; ~~and~~

a co-verification interface comprising a hardware component, a software component modeling the hardware component and being stored on a storage device, or a combination of the hardware and software components; and

a communication system coupling said first and second system elements of the logic design, said first system element being coupled with said communication system and configured to communicate with the second system element via [a] the co-verification interface, comprising:

an application layer having a plurality of communication connections configured to communicate with said first system element;

a network layer in communication with said plurality of communication connections and being configured to select a communication connection from said plurality of communication connections;

a data link layer having a communication connection in communication with said selected communication connection and being configured to communicate with said network layer to provide flow control for said communication connection of said data link layer; and

a physical layer having a communication path in communication with said communication connection of said data link layer and being configured to communicate with said second system element,

wherein the design verification system performs functional verification of the first system element and the second system element, the first system element and the second system element being either a physical system element or a virtual system element, and

wherein the physical system element comprises one or more electronic components and the virtual system element comprises software models of the physical system element.

25. (Currently amended) A method for coupling system elements of a design verification system, comprising:

providing an application layer with a first plurality of communication connections to couple ~~coupling~~ a first system element of the design verification system ~~with a first plurality of communication connections~~ via a first universal coupling interface;

configuring said first plurality of communication connections of the application layer to communicate with said first system element;

providing a network layer in communication with said first plurality of communication connections;

configuring the network layer to select ~~selecting~~ at least one communication connection from said first plurality of communication connections;

providing a data link layer having a communication connection in communication with said at least one selected communication connection;

configuring the data link layer to communicate with said network layer and to provide ~~providing~~ flow control for said at least one communication connection;

providing a physical layer having a communication path in communication with said communication connection of said data link layer; and

transmitting outgoing communication signals from said first system element to a second system element of the logic design via the physical layer ~~said at least one communication connection~~,

wherein the design verification system performs functional verification of the first system element and the second system element of the design verification system, the first system element and the second system element being either a physical system element or a virtual system element, and

wherein the physical system element comprises one or more electronic components and the virtual system element comprises software models of the physical system element.

3. Claims 1-29 are allowable over prior art of record.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HUSSEIN A. EL CHANTI whose telephone number is (571)272-3999. The examiner can normally be reached on Mon-Fri 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571)272-4001. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hussein Elchanti/
Primary Patent Examiner

May 5, 2010